REMARKS

This Amendment is being filed in response to the Office Action mailed February 28, 2007, which has been reviewed and carefully considered. Reconsideration and allowance of the present application in view of the amendments made above and the remarks to follow are respectfully requested.

In the Office Action, claims 1, 4-5, 8 and 11-24 are rejected under 35 U.S.C. §103(a) as allegedly unpatentable over U.S. Patent No. 5,258,968 (Matsuda) in view of .S. Patent No. 6,690,232 (Ueno). It is respectfully submitted that 1, 4-5, 8 and 11-24 are patentable over Matsuda and Ueno for at least the following reasons.

Matsuda is directed to a tracking error signal generating device using a four-segment detector 1. As shown in FIG 18, each segment of the four-segment detector 1 is connected to a buffer amplifier 102. The output of the buffer amplifier 102 is connected to a variable gain amplifier 321 whose output is provided to an adder 104 and fed back to itself (i.e., to the variable gain amplifier 321) through a level detector 325. That is, as clearly shown in FIG 18, the output of the variable gain amplifier 321

itself is fed back to itself (through the level detector 325).

In stark contrast, the present invention as recited in independent claim 1, and similarly recited in independent claims 4-5, 8, 19 and 22, amongst other patentable elements, requires (illustrative emphasis provided):

> at least one slicer for slicing the amplified detection signals to form a sliced output by comparing the amplified detection signals with a reference signal;
> at least one generator in a feedback path between said at least one slicer and said at least one variable gain amplifier for controlling said at least one variable gain amplifier non-linearly... ; and
> a differential time delay detector configured to receive the sliced output and a further input and to detect any time delay between the sliced output and the further input.

It is respectfully submitted that the Matsuda level detector 325 does not receive a reference signal, let alone being able to compare the amplified detection signals with the reference signal. Assuming, arguendo, that the Matsuda level detector 325 is equivalent to the slicer of the present invention as recited in independent claims 1, 4-5, 8, 19 and 22, it is respectfully submitted that Matsuda does not teach or suggest a generator between a slicer and an amplifier. Further, there is no teaching or suggestion in Matsuda of any differential time delay detector

let alone providing the sliced output from the slicer to the differential time delay detector. Ueno is cited to allegedly show other features and does not remedy the deficiencies in Matsuda.

Accordingly, it is respectfully submitted that independent 1, 4-5, 8, 19 and 22 are allowable, and allowance thereof is respectfully requested. In addition, it is respectfully submitted that claims 11-18, 20-21 and 23- should also be allowed at least based on their dependence from independent claims 1, 4-5 and 8.

In addition, Applicants deny any statement, position or averment of the Examiner that is not specifically addressed by the foregoing argument and response. Any rejections and/or points of argument not addressed would appear to be moot in view of the presented remarks. However, the Applicants reserve the right to submit further arguments in support of the above stated position, should that become necessary. No arguments are waived and none of the Examiner's statements are conceded.

In view of the above, it is respectfully submitted that the present application is in condition for allowance, and a Notice of Allowance is earnestly solicited.

Respectfully submitted,

By _____
Dicran Halajian, Reg. 39,703
Attorney for Applicant(s)
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THORNE & HALAJIAN, LLP
Applied Technology Center
111 West Main Street
Bay Shore, NY 11706
Tel: (631) 665-5139
Fax: (631) 665-5101